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Design of an FPGA-Based ECG Signal Analysis System

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Abstract - ECG signals are very small in amplitude and are easily affected by noise, which can make heart-rate measurement and R-peak detection unreliable. In this paper, a real-time ECG acquisition and processing system is developed using the Nexys A7 FPGA to achieve accurate and fast cardiac monitoring. The ECG signal is collected through surface electrodes and conditioned using the AD8232 module, then digitized with the Artix-7 XADC. A 0.5–40 Hz bandpass filter is applied to remove noise and baseline drift. R-peaks are detected using an adaptive thresholding method combined with an exponential moving average and a refractory period, ensuring reliable detection. The heart rate is calculated from RR-intervals and displayed on the onboard 7-segment display, while the processed ECG signal is converted back to analog for oscilloscope observation. The results show that the FPGA-based system provides accurate ECG processing with low delay, making it suitable for portable and embedded cardiac monitoring applications.

Keywords: *ECG, FPGA, AD8232, Heart Rate Detection, Seven-Segment Display, Verilog, Real-Time Monitoring.*

I. INTRODUCTION

Cardiovascular diseases are among the leading causes of death worldwide, which makes continuous monitoring of heart health crucial for early detection and prevention. Electrocardiography (ECG) is a simple and non-invasive technique that records the heart's electrical activity, helping doctors understand its rhythm and overall function. Traditional ECG devices, such as those used in hospitals, are often bulky, expensive, and not suitable for continuous monitoring outside clinical settings.

With recent advancements in digital electronics and embedded systems, it is now possible to develop portable, low-power, and real-time heart monitoring solutions. Field Programmable Gate Arrays (FPGAs) are particularly well-suited for such biomedical applications due to their ability to perform multiple tasks simultaneously, process data quickly, and allow flexible implementation of custom signal processing algorithms.

In this paper, we present an FPGA-based ECG monitoring system that uses the AD8232 ECG sensor to capture heart signals and a Xilinx FPGA to process them in real time. The system calculates and displays the user's heart rate on a seven-segment display, providing instant feedback about cardiac health. By using FPGA technology, the design ensures fast and accurate heartbeat detection while keeping hardware usage efficient. This approach offers a portable, affordable, and reliable solution for continuous heart monitoring, making it suitable for both hospital and home use.

II. Related Work

Despite the rapid advancement of ECG monitoring systems in recent years, achieving a solution that is simultaneously real-time, accurate, and portable remains a significant challenge. Conventional systems often face difficulties in handling noise in ECG signals, dealing with latency during signal processing, and overcoming hardware limitations that restrict deployment outside clinical environments. These limitations make continuous cardiac monitoring in home or ambulatory settings difficult, emphasizing the need for efficient, low-latency, and reliable embedded solutions.

Smith and L. Johnson [1] developed an FPGA-based arrhythmia detection system that combines preprocessing, wavelet-based feature extraction, and machine learning classification. Their system successfully detects arrhythmias in real time with high accuracy, demonstrating the benefits of implementing signal processing and classification directly on FPGA hardware. However, the study also highlighted that hardware resource optimization is critical, as the FPGA must

efficiently handle multiple processing tasks simultaneously to maintain performance. M. Al-Salami et al. [2] provided a comprehensive review of FPGA-based ECG classification techniques, summarizing approaches that include digital filtering, parallel computation, and machine learning algorithms.

Their review emphasized the advantages of FPGA platforms, such as deterministic execution and high-speed processing, but also highlighted challenges such as hardware constraints and sensitivity to noise in ECG signals.

A. Rahman and M. Hussain [3] proposed an FPGA implementation of IIR elliptic filters to remove baseline wander and high-frequency noise from ECG signals. Their approach ensures that the ECG waveform is clean and suitable for accurate heart-rate detection, while maintaining low-latency, real-time operation and low power consumption. In a similar effort, S. Kumar et al. [4] implemented wavelet-transform-based algorithms on FPGA to detect QRS complexes and measure heart rate in real time. The system was shown to be robust against noise and signal variability, highlighting the potential for FPGA systems in wearable and portable monitoring devices. On the other hand, Arpita Paul et al. [5] focused on software-based approaches using support vector machines (SVM) and deep learning for arrhythmia detection. While their method achieved high detection accuracy, it primarily relied on pre-filtered ECG data and lacked real-time hardware implementation, showing the importance of bridging algorithmic efficiency with embedded deployment.

J. Lee and M. Park [6] proposed a dual-function FPGA accelerator that combines one-dimensional convolutional neural networks (1-D CNNs) for ECG classification with heart-rate estimation. This design mapped the entire processing chain onto FPGA hardware, achieving low-power, real-time operation suitable for wearable monitoring devices. N. Prasad et al. [7] implemented neonatal ECG monitoring on an FPGA, demonstrating reliable extraction of heart rate with low latency and efficient power usage, emphasizing the suitability of FPGA hardware for sensitive biomedical applications. R. Das et al. [9] focused on preprocessing modules for low-power ECG denoising, showing that real-time FPGA implementation of signal cleaning significantly improves the accuracy of subsequent heart-rate and arrhythmia detection.

Several studies have also explored wearable and portable ECG monitoring devices. Reviews by Y. Zhang and P. Liu [11,14] highlighted the integration of polymer-based ECG sensors with FPGA processing units to achieve accurate, portable, and patient-friendly monitoring solutions. L. Gomez et al. [12] presented a lightweight temporal convolutional network for arrhythmia detection on wearable devices, demonstrating the feasibility of adapting such algorithms to FPGA hardware for real-time analysis with low computational resources. R. K. Sharma et al. [13] proposed an edge-fog-cloud architecture for continuous ECG monitoring, combining local real-time preprocessing with cloud-based analytics. Their work emphasizes low-power operation, real-time constraints, and scalability for multiple patients. Finally, N. Prasad et al. [15] implemented a heart rate detection system using counters and comparators on FPGA, achieving accurate, low-latency measurements. Their approach closely resembles the methodology of the present work, reinforcing the practical feasibility of FPGA-based solutions for continuous cardiac monitoring.

In summary, these studies collectively demonstrate the significant potential of FPGA-based ECG monitoring systems. FPGAs enable high-speed parallel processing, deterministic operation, energy efficiency, and the ability to integrate preprocessing, feature extraction, and classification in a single hardware platform. However, limitations remain in terms of hardware resource utilization, robustness against signal noise, and fully portable designs for home-based or wearable applications. These challenges highlight the need for a cost-effective, reliable, and real-time FPGA-based ECG monitoring system capable of continuous operation, which forms the basis and motivation for the present work.

III. METHODOLOGY

The proposed system is designed to acquire, process, and visualize ECG signals in real time, integrating both hardware and software components for efficient performance. ECG electrodes first detect the heart's electrical activity and generate continuous analog signals. These signals are fed into the XADC module of the Artix-7 FPGA, where they are converted from analog to digital form. The FPGA executes Verilog-based digital signal processing, beginning with a low-pass filter that removes high-frequency noise and baseline drift while preserving the essential features of the ECG waveform. After filtering, the system performs R-peak detection, identifying the peaks necessary for accurate heart rate calculation. Using the detected peaks, the real-time heart rate is computed and stored. The processed digital signal is then sent to the DAC0800 module, converting it back to analog for display purposes. The analog ECG waveform is finally displayed on an oscilloscope, enabling real-time observation of cardiac activity. This methodology ensures precise signal acquisition, robust digital processing, and accurate visualization. The integration of hardware and software allows simultaneous monitoring and analysis, supporting both clinical and research applications. By combining FPGA-based processing with real-time analog output, the system achieves high reliability and minimal latency. The approach is scalable and can be adapted to include additional features like data logging or wireless transmission in future developments. Overall, the proposed methodology provides

a complete framework for real-time ECG monitoring and heart rate computation with high accuracy and efficiency.

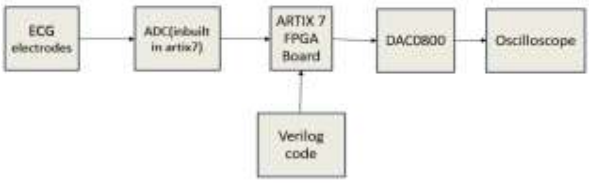


Figure 1: Block diagram of Design of FPGA Based ECG Signal Analysis System

The Figure 1 shows the block diagram of a Design of FPGA based ECG signal analysis system, in which the complete flow of signal acquisition, processing, and visualization is clearly illustrated. The process begins at the biosensing stage, where conductive ECG electrodes are placed at specific anatomical locations on the chest to detect the electrical activity produced by the heart. These electrodes sense the minute voltage variations generated during the depolarization and repolarization of cardiac muscle tissues. Since the ECG signal amplitude typically lies in the millivolt range, it is highly sensitive to disturbances such as motion artifacts, poor electrode contact, skin impedance fluctuations, and environmental electromagnetic noise. To enhance signal quality, appropriate skin preparation methods such as cleaning, mild abrasion, and the application of conductive gel are employed. The electrodes convert the physiological ionic currents into measurable electrical signals, forming the primary input to the system.

The acquired analog ECG signal is then directed to the inbuilt Analog-to-Digital Converter (ADC) of the Artix-7 FPGA board. This ADC performs the essential task of converting the continuous-time analog waveform into a discrete digital format through sampling and quantization. Critical parameters such as ADC resolution, sampling frequency, and voltage range significantly affect the accuracy and fidelity of the digitized signal. A higher resolution ensures finer amplitude representation, while an adequate sampling rate prevents aliasing and preserves waveform integrity.The digital representation allows the ECG signal to be effectively processed by the FPGA's internal logic resources.

Once digitized, the ECG data is processed within the Artix-7 FPGA using Verilog-based signal processing modules. These modules implement various digital filters, including low-pass, high-pass, and notch filters, to eliminate baseline drift, power line interference, and muscular noise. Additional processing blocks perform peak detection and QRS complex identification to extract vital cardiac parameters such as heart rate and rhythm regularity. The FPGA's parallel processing and pipelined architecture enable real-time computation with minimal delay, ensuring efficient and accurate signal enhancement. This stage refines the waveform while retaining essential diagnostic characteristics.

In the final stage, the processed digital signal is passed to the DAC0800, which reconverts the digital data into an equivalent analog voltage signal. This reconstructed waveform is then supplied to an oscilloscope for real-time visualization. The oscilloscope displays the ECG waveform, allowing observation of key morphological features such as P-waves, QRS complexes, and T-waves. This visual output serves as a confirmation of the system's performance and accuracy. Thus, the complete methodology demonstrates a seamless integration of biological signal acquisition, digital processing using FPGA technology, and analog display for reliable ECG signal analysis.

IV. IMPLEMENTATION

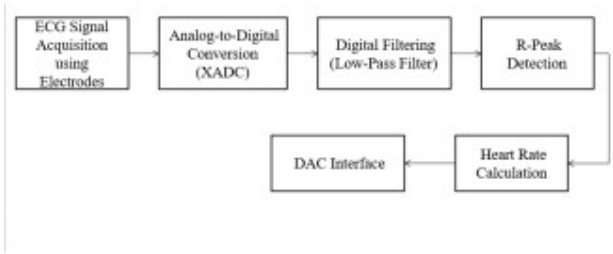


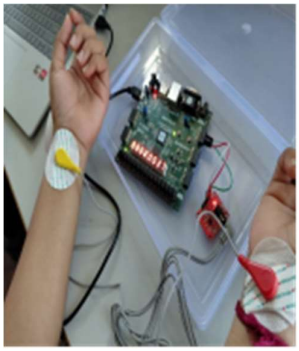
Figure 2: Flow of Implementation Using Vivado

The flow begins with ECG signal acquisition using electrodes, which capture the minute electrical impulses generated by cardiac activity. These raw analog signals are first conditioned by the ECG sensor module and then supplied to the FPGA for further processing. Since the native signal is continuous in nature, it cannot be directly handled by digital logic. Therefore, this stage focuses on obtaining a stable and measurable representation of the ECG waveform that accurately reflects the physiological activity of the heart.

The acquired analog signal is then routed to the XADC (Xilinx Analog-to-Digital Converter) embedded within the Artix-7 FPGA. The XADC converts this time-varying analog signal into discrete digital samples by performing periodic sampling and quantization. This conversion enables the FPGA to interpret the ECG signal in binary form, allowing precise numerical manipulation. Proper sampling frequency and resolution ensure that critical features of the ECG waveform are preserved without distortion or loss of information.

Once digitized, the signal is passed through a digital low-pass filter implemented in Verilog. This filtering stage plays a crucial role in minimizing unwanted noise such as baseline drift, high-frequency interference, and motion-related disturbances. By allowing only the essential frequency components associated with ECG activity to pass through, the filter enhances waveform clarity and improves the reliability of further analysis procedures.

The filtered signal is then analysed using an R-peak detection module. This block identifies the most prominent spike in the ECG waveform, which corresponds to ventricular contraction. Accurate detection of R-peaks is essential because it forms the basis for calculating



temporal intervals between heartbeats. Following this, the heart rate calculation module determines the beats per minute (BPM) by measuring the time difference between successive R-peaks.

Finally, the processed digital ECG signal is routed through the DAC interface block. This module controls the DAC0800, converting the digital waveform back into an analog signal for visualization. The reconstructed signal is displayed on the oscilloscope, allowing real-time observation of the ECG pattern. This stage confirms that the entire processing chain—from acquisition to analysis and reconstruction—operates correctly and produces a clinically interpretable waveform.

V. RESULTS AND DISCUSSIONS

The successful simulation demonstrates the FPGA-based ECG Signal Analysis System designed for real-time heartbeat detection and heart rate monitoring. The complete system is implemented using Verilog HDL and verified on an FPGA platform. All major functional modules—including ECG signal acquisition, filtering, R-peak detection, and beats-per-minute (BPM) calculation—are integrated into a single cohesive design, ensuring reliable and accurate signal processing.

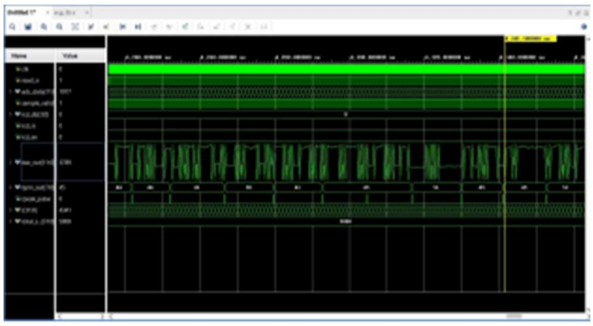
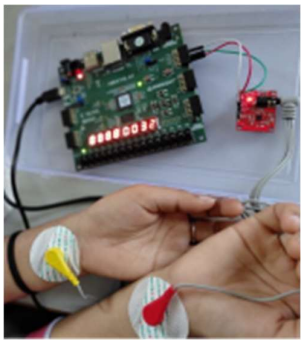


Figure 3: ECG Signal Processing Simulation Output

Figure 1 shows the simulated waveform of the FPGA-based ECG Analysis System. The design, written in Verilog HDL, was tested using a waveform viewer to check how the system reads the raw ECG signal, detects R-peaks, and calculates the heart rate in real time. The top signals, like clock and reset, keep the system synchronized. The adc_data signal represents the ECG samples from the ADC, and sample_valid shows when each new sample arrives. After processing, the dac_out signal displays a cleaner and amplified ECG waveform. The R-peaks are clearly visible as sharp pulses in the rpeak_pulse signal. The heart rate is shown in bpm_out, which updates automatically with each detected beat. Overall, the simulation confirms that the FPGA correctly filters the signal, identifies heartbeats, and calculates BPM as expected.



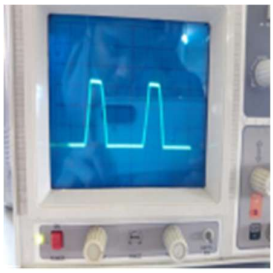
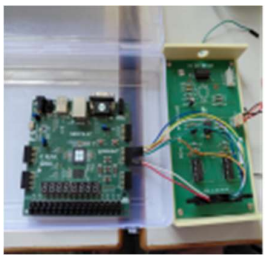


Figure 4: AD8232 ECG Front-End Module and Its Oscilloscope Output

The AD8232 module was used to collect the heart's electrical signals and clean them before sending the data for digital processing. It has built-in amplification and filtering, which helps remove noise and gives a smooth and clear ECG waveform. To make sure the module was working properly, its output was checked on an oscilloscope. The waveform appeared clear and stable, showing that the sensor was correctly capturing the heart's activity. This testing confirmed that the system can provide reliable ECG data to the FPGA for further steps like filtering, R-peak detection, and heart rate calculation.



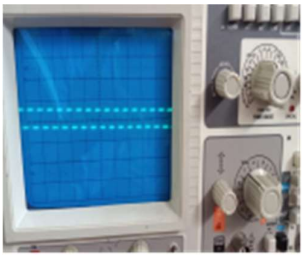


Figure 5– Interfacing of FPGA (Artix-7) with External DAC Module and Observation of Analog Output on CRO

This setup shows how the DAC module is connected to the Nexys A7 (Artix-7) FPGA board to create analog waveforms that can be viewed on an oscilloscope. The FPGA sends out digital values—usually 8-bit data—through its GPIO pins to the DAC board. The DAC then converts these digital numbers into matching analog voltage levels. This analog output is

connected to the oscilloscope so the waveform can be seen in real time.

By changing the digital pattern inside the FPGA—like using a counter, ramp signal, or lookup-table-based design—you can generate different types of waveforms such as sawtooth, triangle, square, or sine waves. In your oscilloscope image, the dotted steps show a staircase-like signal, which is typical of a counter running at a lower sampling rate. Adjusting the time/div, volts/div, and trigger settings on the CRO helps make the waveform smoother and clearer.

Figure 6: FPGA-Based ECG Monitoring Setup with Seven-Segment BPM Display

Figure 4 shows the live testing setup of the ECG monitoring system. ECG electrodes are attached to the subject's arms and connected to the AD8232 module, which captures and cleans the heart signal. This signal is then sent to the FPGA,

where the ECG processing logic—filtering, R-peak detection, and BPM calculation—runs in real time. The BPM values are shown on the seven-segment display of the Nexys A7 FPGA board. The images confirm that the system is able to read the heart signal correctly and update the heart rate continuously, proving that the hardware and processing algorithm work reliably during real-time use.

VI. CONCLUSION AND FUTURE WORK

This paper successfully put forth a real-time FPGA-based ECG monitoring and heart-rate detection system using the Nexys A7 FPGA and AD8232 analog front-end, achieving accurate ECG acquisition, digital filtering, adaptive R-peak detection, and reliable heart-rate calculation even in noisy conditions. The system's compact and user-friendly design, with heart-rate display on a 7-segment module and validation through DAC-based analog reconstruction, ensured high-speed, low-latency, and energy-efficient performance suitable for portable medical devices. Its modular architecture allows future enhancements such as multi-lead ECG acquisition, wireless connectivity for remote monitoring, FPGA-based machine learning for arrhythmia detection, mobile and cloud integration, additional bio signal sensing, power optimization for wearables, and emergency alert features, enabling the evolution of the system into an intelligent, autonomous, and scalable cardiac healthcare platform.

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